High Speed Magnetic Pulse Generator

Final Review Presentation

Team May1740

Jack Lamar

Qibai Zheng

Ran Ma

Pengchao Lian

Advisers

Dr. Mani Mina

Jayaprakash

Last edited: 4.24.17

Project Introduction

Context

Magneto Optic switching in fiber optic network routing

Problem Statement

Previous work on the MO switching circuit has led to satisfactory switching characteristics. However, we believe there is much work left to be done in further optimization and tailoring to specific applications.

Past Work

- Over the past couple years, senior design teams and research teams have worked on this project
- Last semester: Project Fundamentals
  - Learn context of the project
  - Understand fundamentals of their circuit: purpose of each component, reasoning for component values, etc.
- This semester: New Design Ideas
  - Identify areas of improvement
  - Brainstorm and design solutions for improvement
  - Test solutions
  - Make recommendations for future work

Project Requirements

Functional

- Output:

  $B \geq 500\ Gauss$

  $Rise\ Time\ < 100\ ns$

- Transmitting coil must fit fiber optic connection:

  $Diameter\ \geq 4\ mm$

Non-Functional

- Output must be consistent
- Board must have structural integrity for long term use (soldering, components, etc.)
- $PCB\ Size\ \leq 3.5" \times 2"$

Software and Hardware

Software

- NI Multisim 14.0
  - Used to model and simulate circuit
- NI Ultiboard 14.0
  - Used to design circuit layout
- MATLAB
  - Used to model theory of low power design
- Eagle 7.7
  - Used to do circuit layout for fitting ISU ECpE PCB cutter.

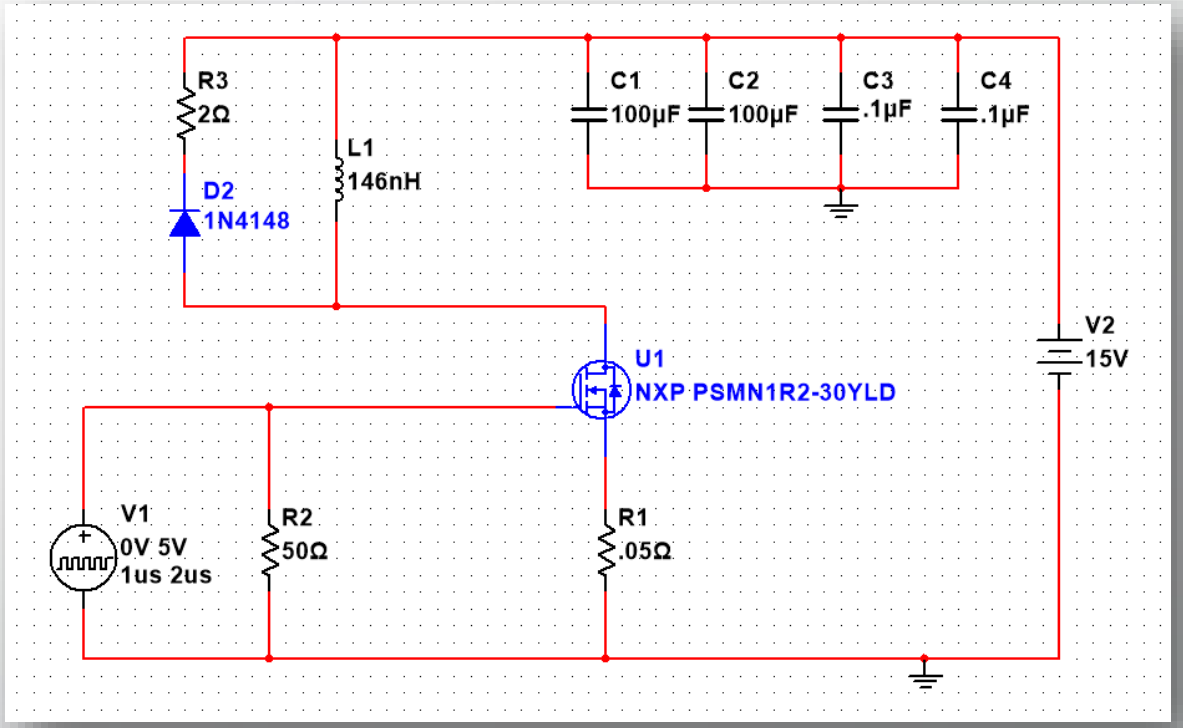
Hardware

- Tektronix AFG 3021B function generator
- Agilent E3631A DC power supply
- Tektronix DPO 4032 Oscilloscope
- 50 ohm coaxial cables
- Handheld multimeter
- ISU ECpE board fabrication drill

Circuit Fundamentals

Components

- ***MOSFET*** – controls and amplifies current flow through the inductor
- ***Inductor*** – used to transmit the magnetic field pulse
- ***Capacitors*** – bank used to store enough energy to empty through the coil in order to achieve desired current
- ***Resistors*** –
  - R1 – used as current-sense resistor and limits current
  - R2 – matches the output impedance of the pulse source
  - R3 – absorbs excess energy in feedback loop
- ***Pulse Source*** – controls the FET gate which determines timing of current pulse
- ***DC Source*** – generates energy to be stored in capacitors and sent through the inductor
- ***Diode*** – controls current flow in feedback loop



New Design Plan

- Idea 1: new location for current-sense resistor
  - Design new board to measure current through inductor in more direct way
  - Goal: more accurate measurement and better results
- Idea 2: test new MOSFETs
  - Theory: increase channel resistance to decrease rise time (t = L/R)
  - Research new MOSFET possibilities (higher R_{on}, lower C_{input})

Idea 1: Current-Sense Resistor

Overview

Main idea

For observing and testing needs, we have to add some device to make it be able to observe and test the current change of inductor. Last group used a 0.05ohms resistor to work as the current-sense device. And we build our new board with two 0.05Ω resistors on the two side of the MOSFET. And we made the circuit as right side shown.

Idea 1: Current-Sense Resistor

Testing Results

	Original circuit current sensor	New current sensor
Rise time	292.5ns	97.0ns
Amplitude	21.2V	24.1V
Tuning	Yes	Not obvious
Graph	Figure 1	Figure 2

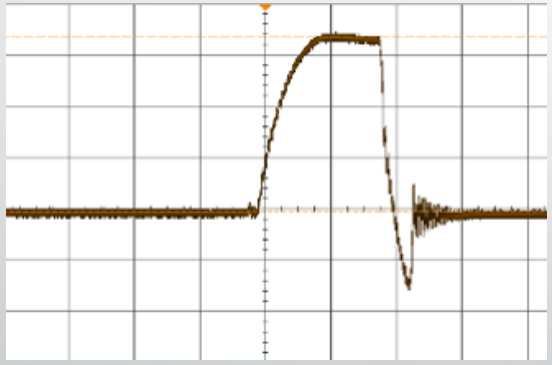


Figure 1

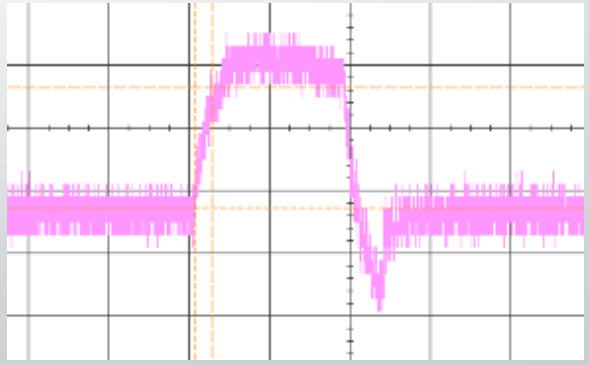
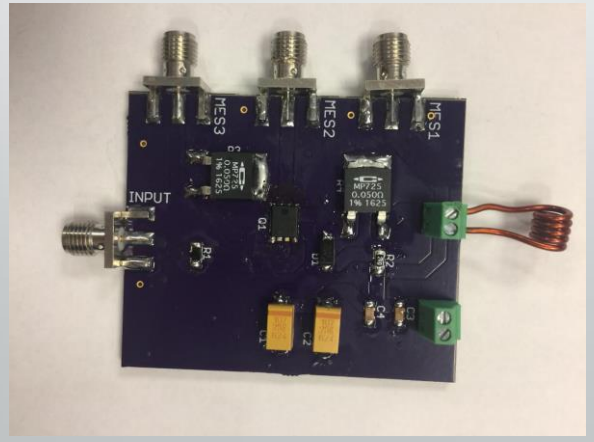


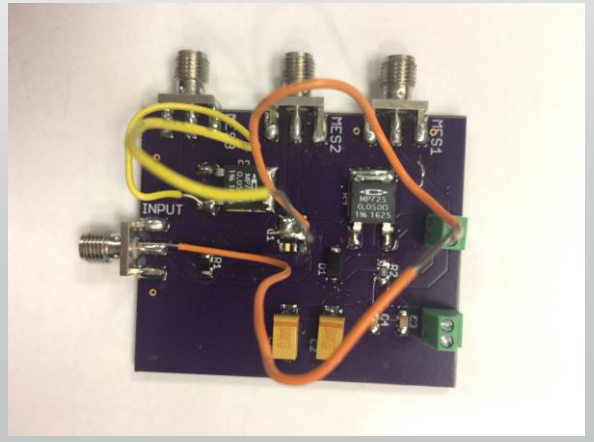
Figure 2

Idea 2: New MOSFET Options

Overview

- A higher resistance and lower input capacitance MOSFET
- To obtain a shorter rise time based on the theory t = L/R =RC
- We created two types of testing boards:
  - Solder-Version
    - For the smaller surface-mount FETs
  - Wire-Version
    - For the larger through-hole FETs





Idea 2: New MOSFET Options

Testing Results

MOSFET	Input Capacitance	ON Resistance	Amplitude	Rise/Fall Time	Connection Type	Result
CSD 17507Q5A	0.41nF	20mΩ	15.7V	9.5ns	Soldered	Figure 1
CSD 18542KCS	3.9nF	10mΩ	9.6V	756ns	Wired	Figure 2
CSD 18563Q5A	1.15nF	>25mΩ	16.5V	80ns	Soldered	Figure 3

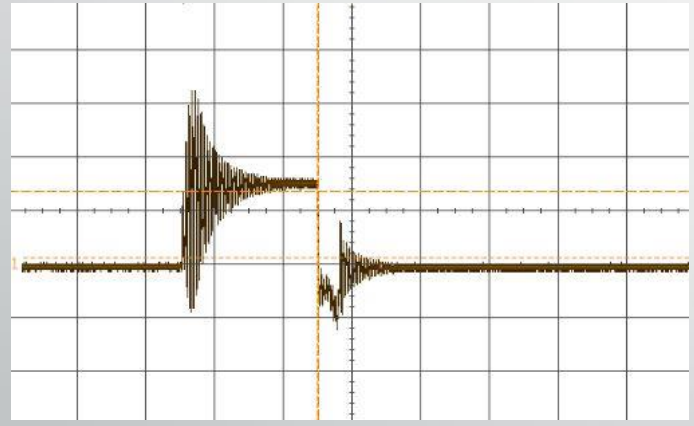


Figure 1

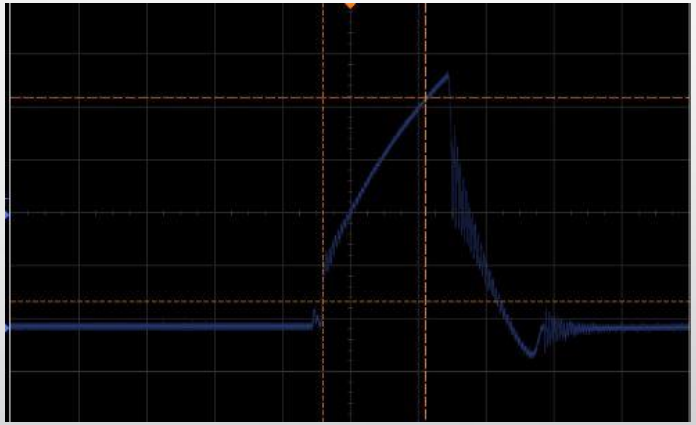


Figure 2

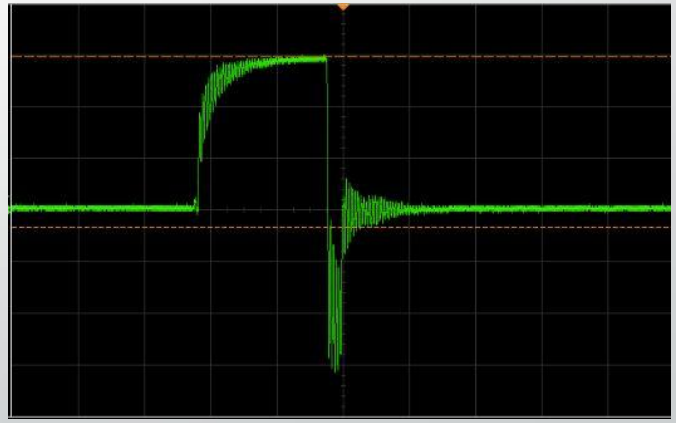


Figure 3

Design Challenges

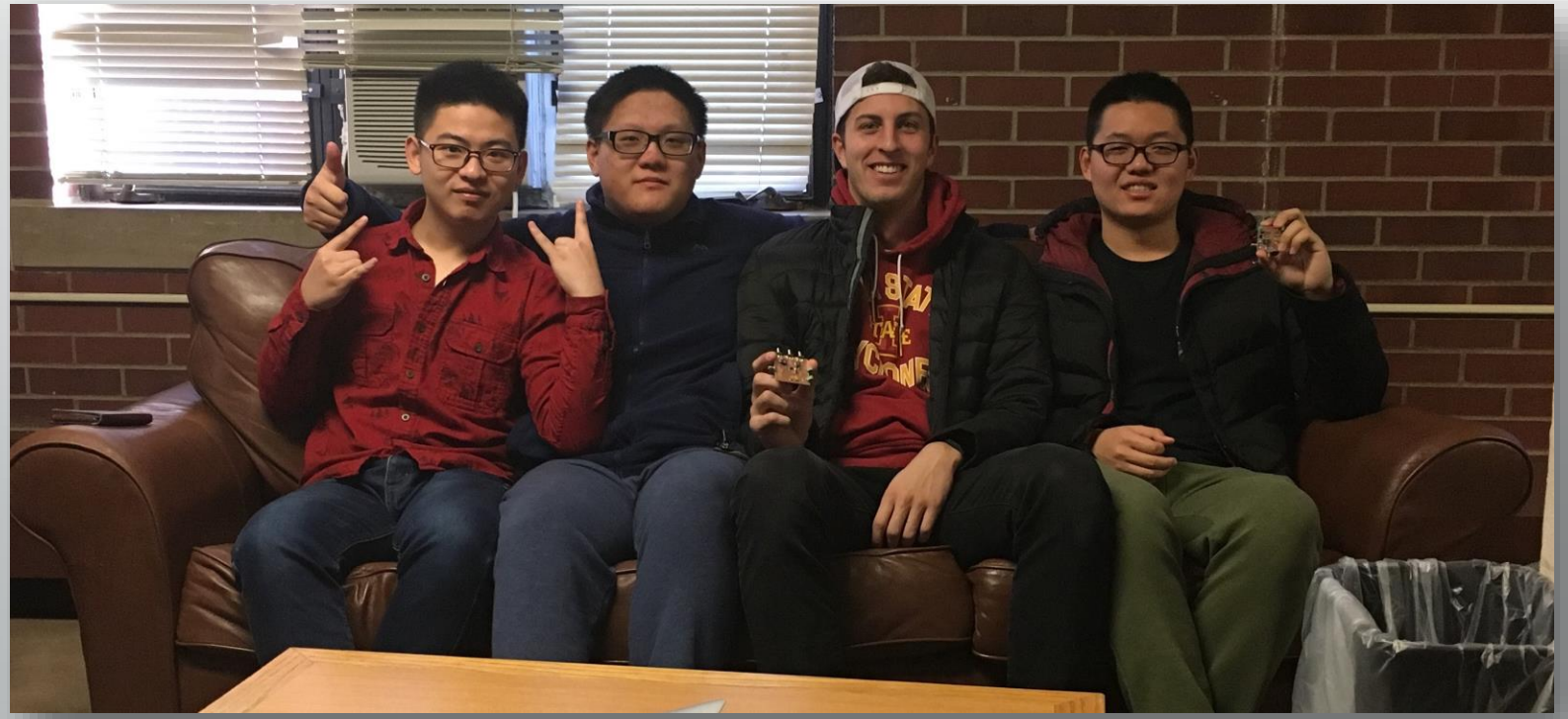
- Throughout the design process we came across various challenges:
  - Inductance measurement: calculating theoretical inductance (equations) showed very different values than experimental inductance (testing)
  - Compounding effects of circuit changes: tradeoff between rise time and output magnitude
  - MOSFET research: Parameters are complicated. We only focused on R_{on} and C_{input}, but other factors could be influencing our results

Recommendations for Future Work

- Lowpass filter out high frequency noise (ringing) to get more accurate results
- Test other current-sensing resistor options (higher resistance and power rating)
- Continue testing on new MOSFETs
- Move deeper into fall time testing

Team Breakdown

- Qibai Zheng – specialized in layout design and fabrication
- Ran Ma – specialized in website and layout design
- Pengchao Lian – specialized in testing and measurement
- Jack Lamar – team leader



Thank You

Questions?

Backup Slides

Future Plans – Low Power Design

Main Idea

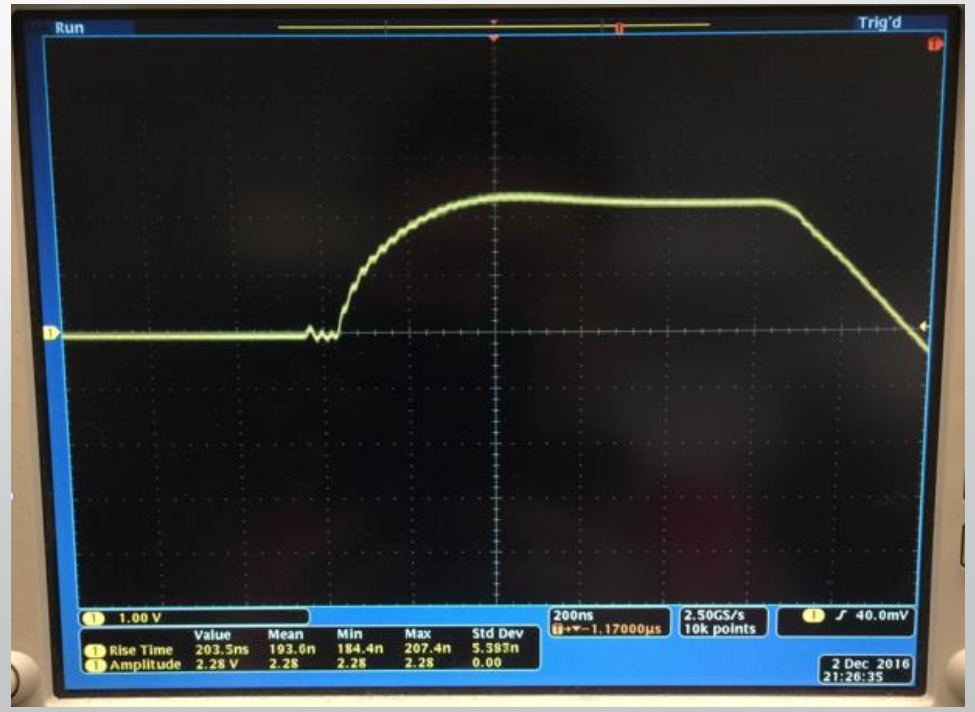
Find an optimized (lower) level of current to send through the coil in order to achieve a 500 gauss peak B-field within an acceptable rise time. This will require making modifications to the current circuit.

- **Base Equations:** $\tau = \frac{L}{R}$ $B = \frac{\mu N I}{\sqrt{l^2+4R^2}}$ $L = \frac{\mu N^2 A}{\sqrt{l^2+4R^2}}$
- **Calculations:** $L = \frac{\mu N^2 A}{\sqrt{l^2+4R^2}} \rightarrow \frac{\mu N}{\sqrt{l^2+4R^2}} = \frac{L}{NA} \rightarrow B = \frac{LI}{NA} \rightarrow L = \frac{BNA}{I} \rightarrow \boldsymbol{\tau = \frac{BNA}{IR}}$
- **Conclusion:** 1. $const\ \tau = \frac{500(NA)\downarrow}{I\downarrow\ R}$ 2. $const\ \tau = \frac{500NA}{I\downarrow\ R\uparrow}$ 3. $const\ \tau = \frac{500NA\downarrow}{I\downarrow\ R\uparrow}$

PCB Testing and Measurement

In order to find out the suitable value for the inductance for a short rise time, we would like to test in different coils. And the following chart showed is two group of data we tested:

Numbers of Turns	Loop Diameters	Wire Diameters	Length of Coil	Inductance of Coil	Rise time	Amplitude
5	5mm	0.92mm	6mm	139nH	252ns	2.39V
3	5mm	0.92mm	3mm	50nH	193ns	2.25V

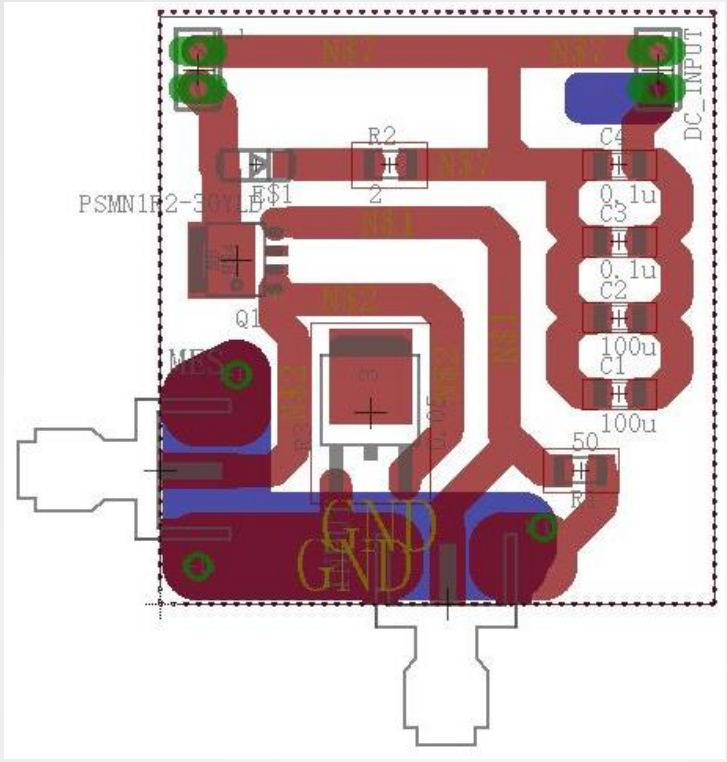


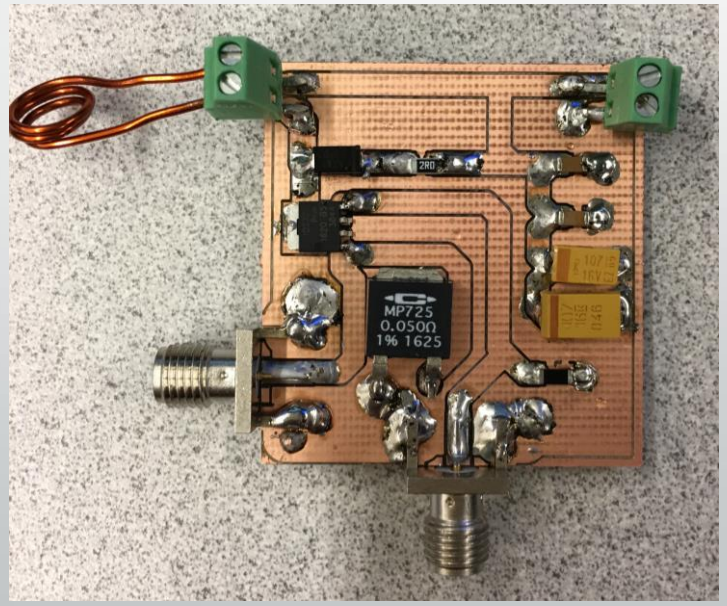
PCB Fabrication

Eagle PCB Design 7.7

Gerber Files

Board Fabrication Machine

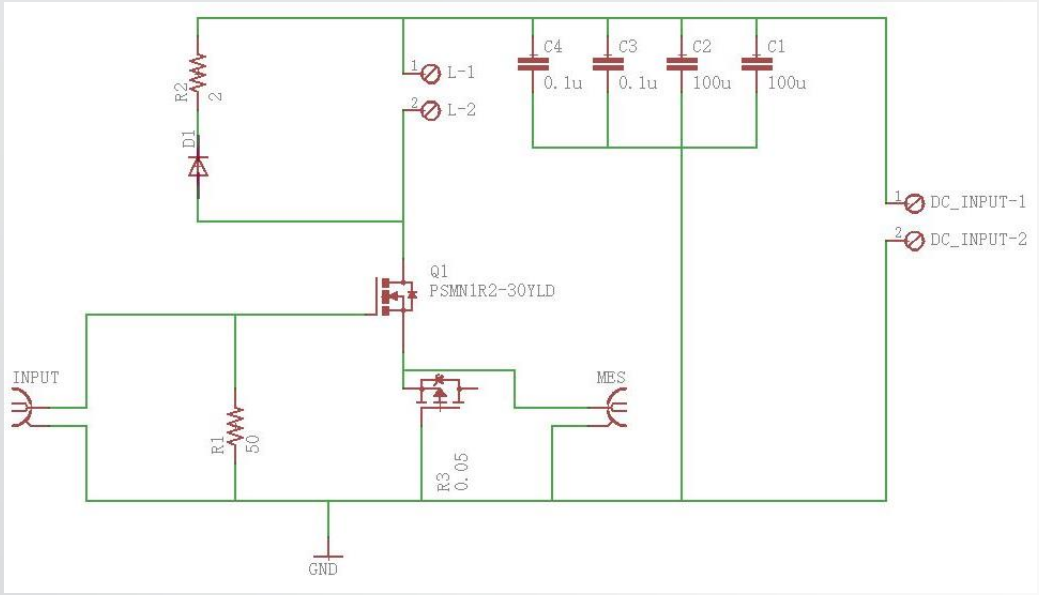


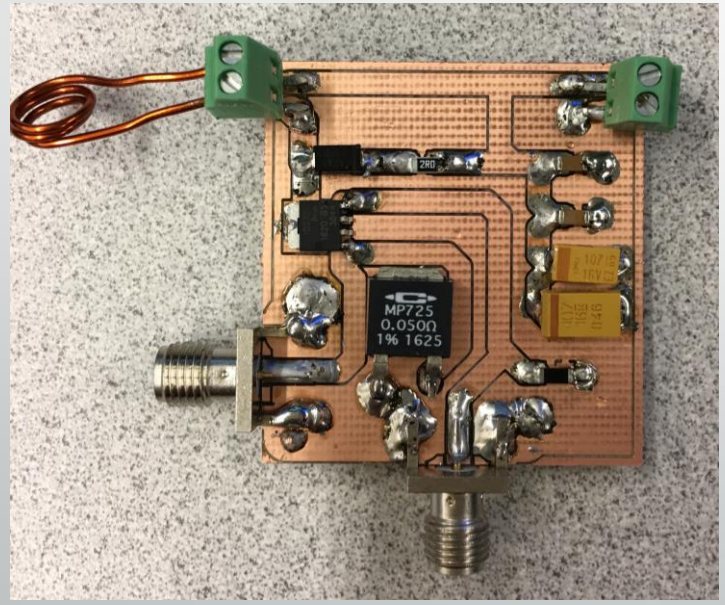


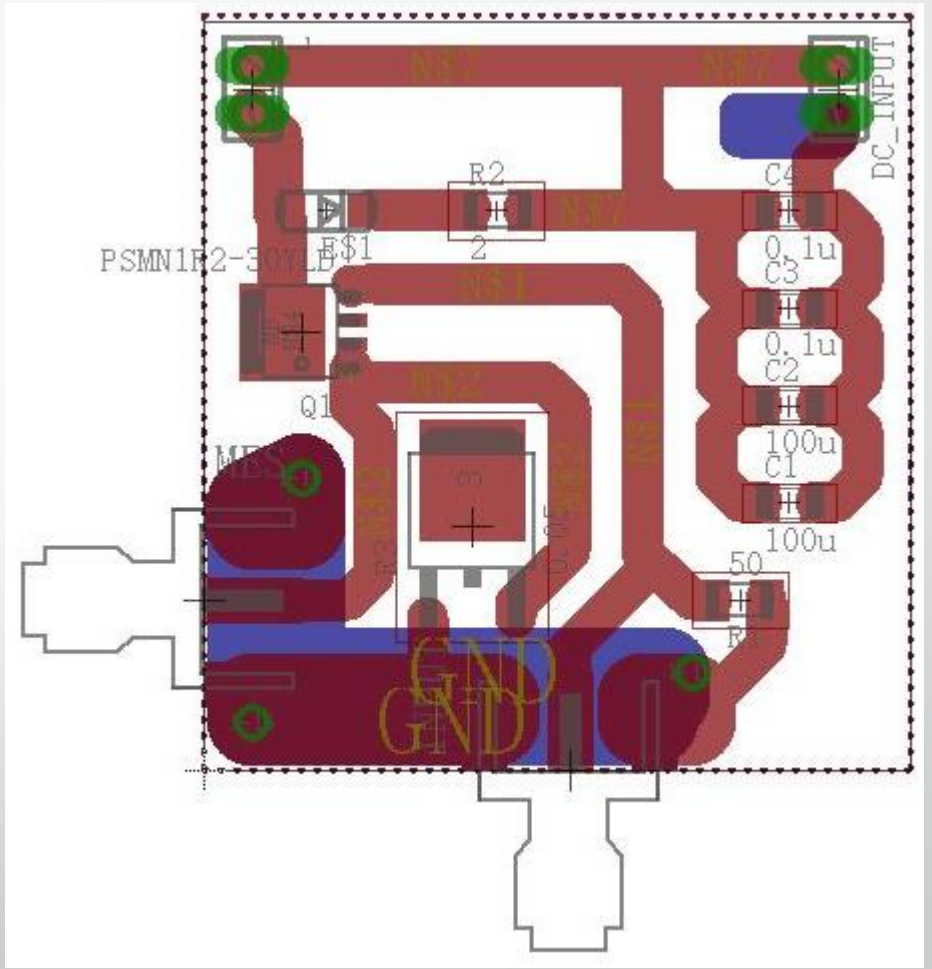
Parts

- 2 *Terminal Blocks
- 2 *SMA connectors
- 2 *0.1µF Capacitors in 1206 package
- 2 *100µF Capacitors in 1206 package
- 1 *50 Ω Resistor in 1206 package
- 1 *2 Ω Resistor in 1206 package
- 1 *0.05 Ω Power Film Resistor
- 1* MOSFET PSMN1R2-30YLD
- 1 * Diode in DO-214AC package

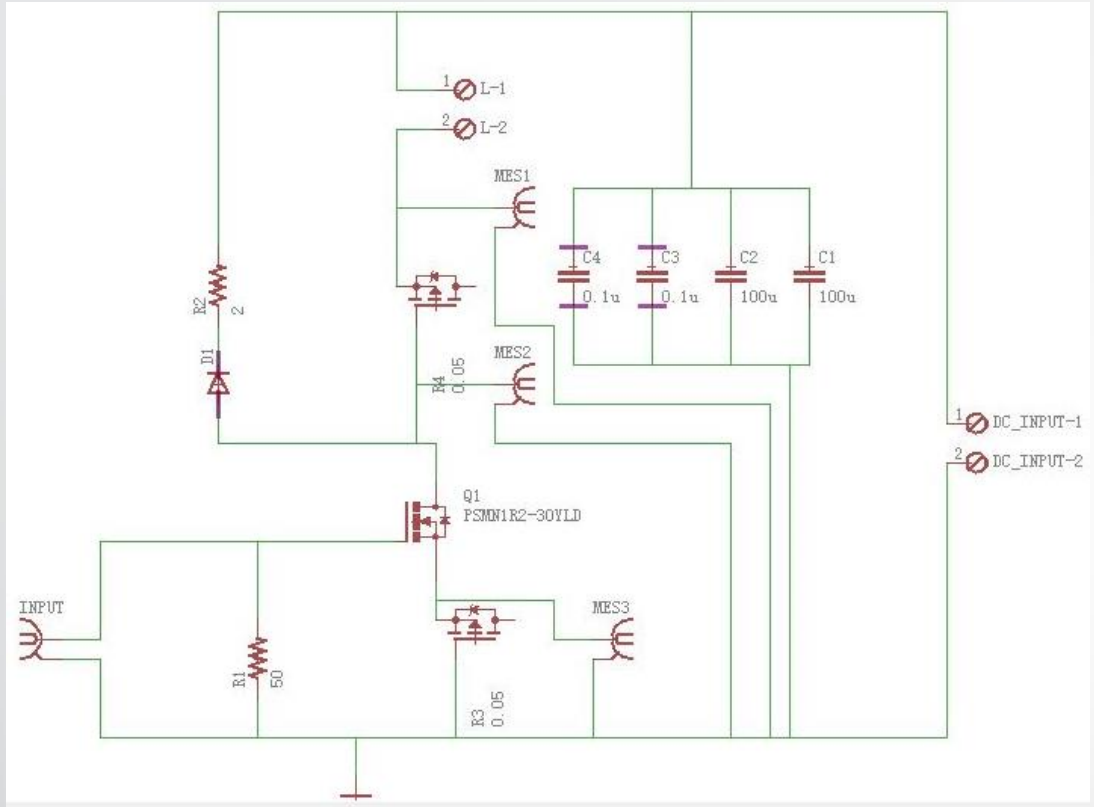
Circuit Board 1

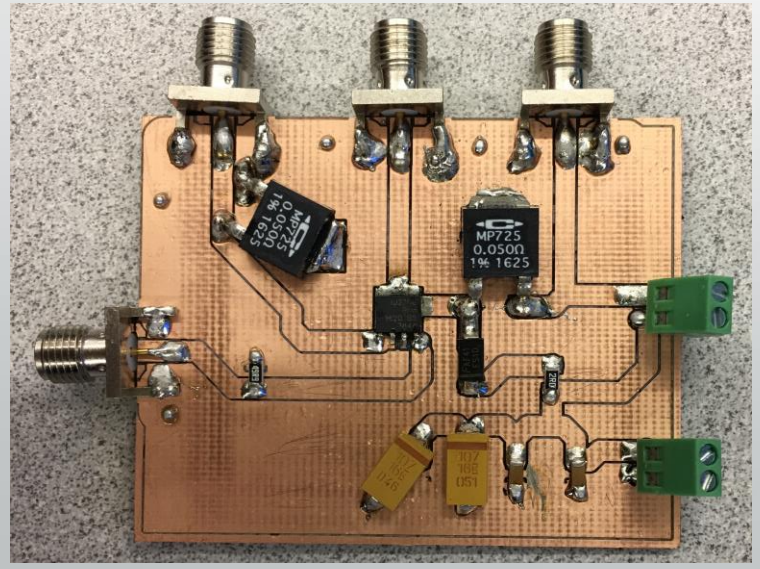


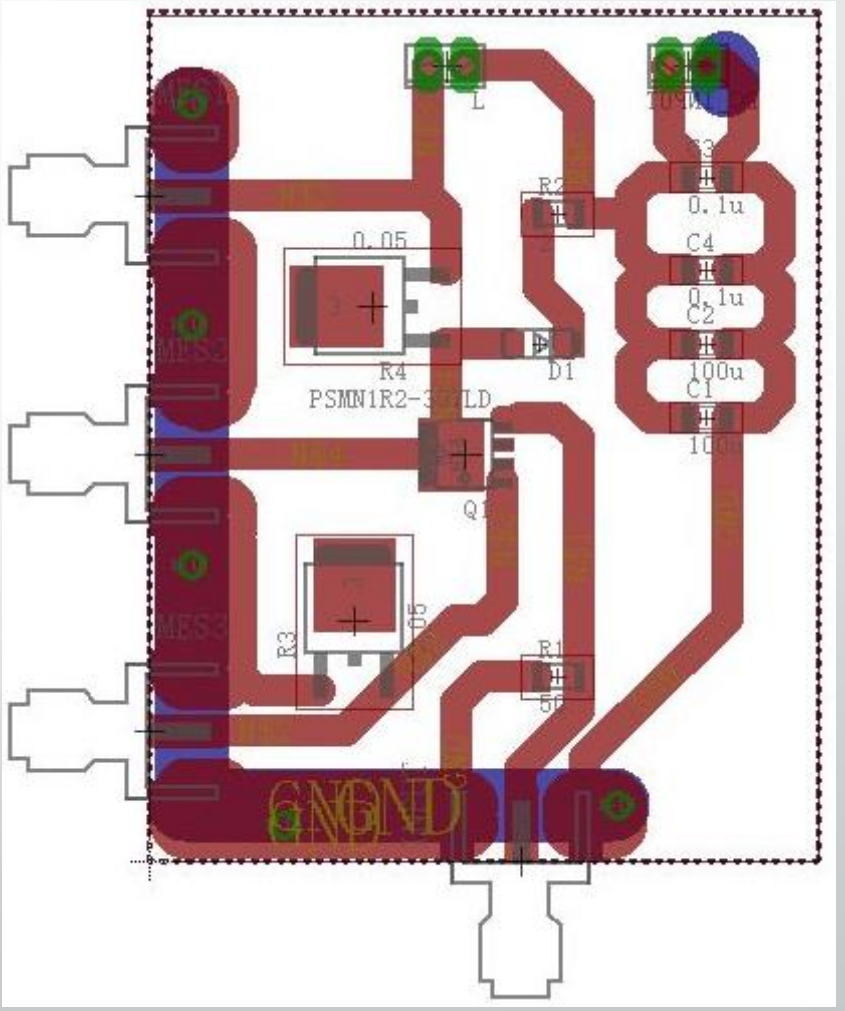




Circuit Board 2

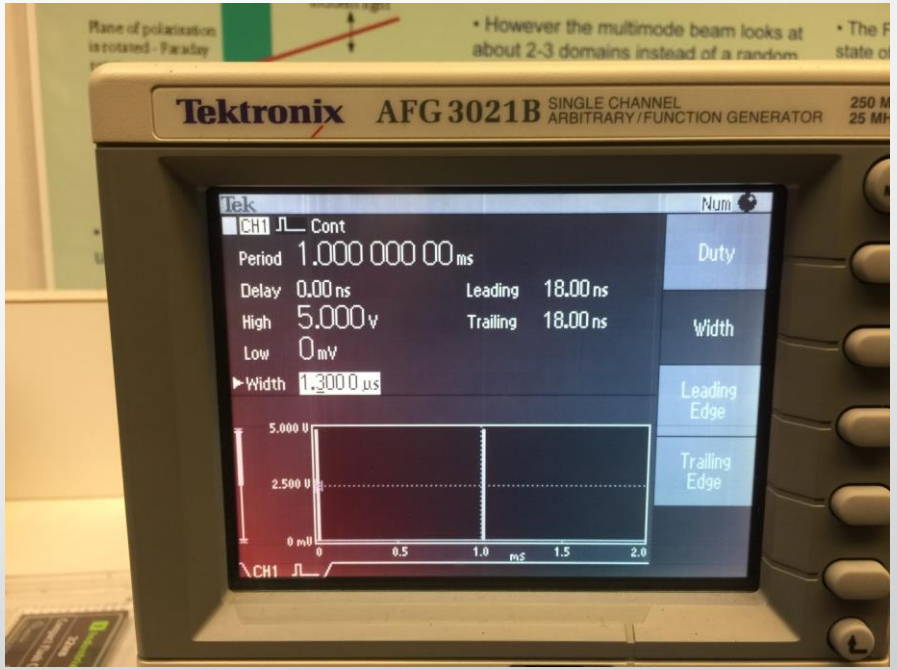






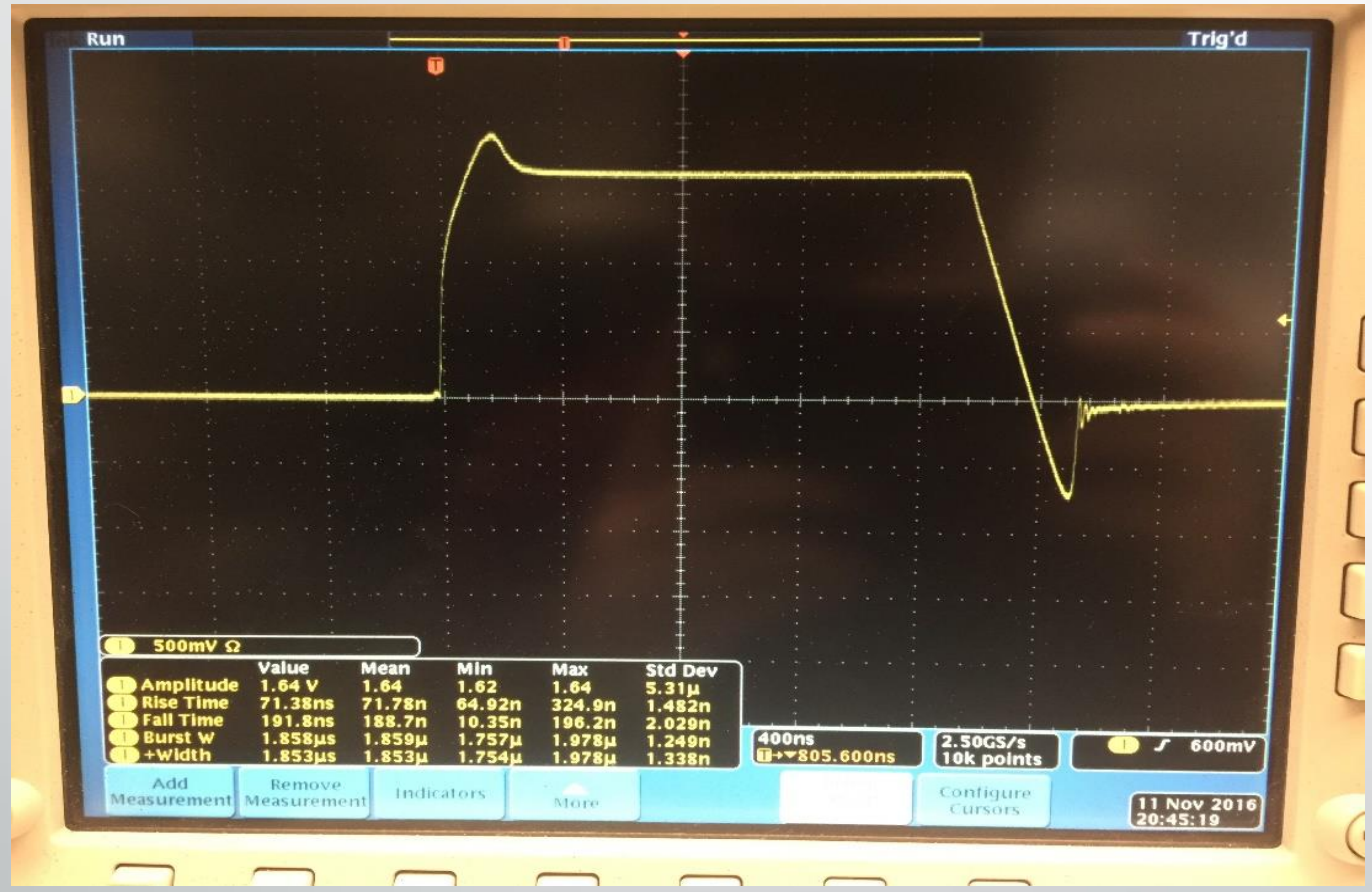
Measurement setting up

Power supply setting up



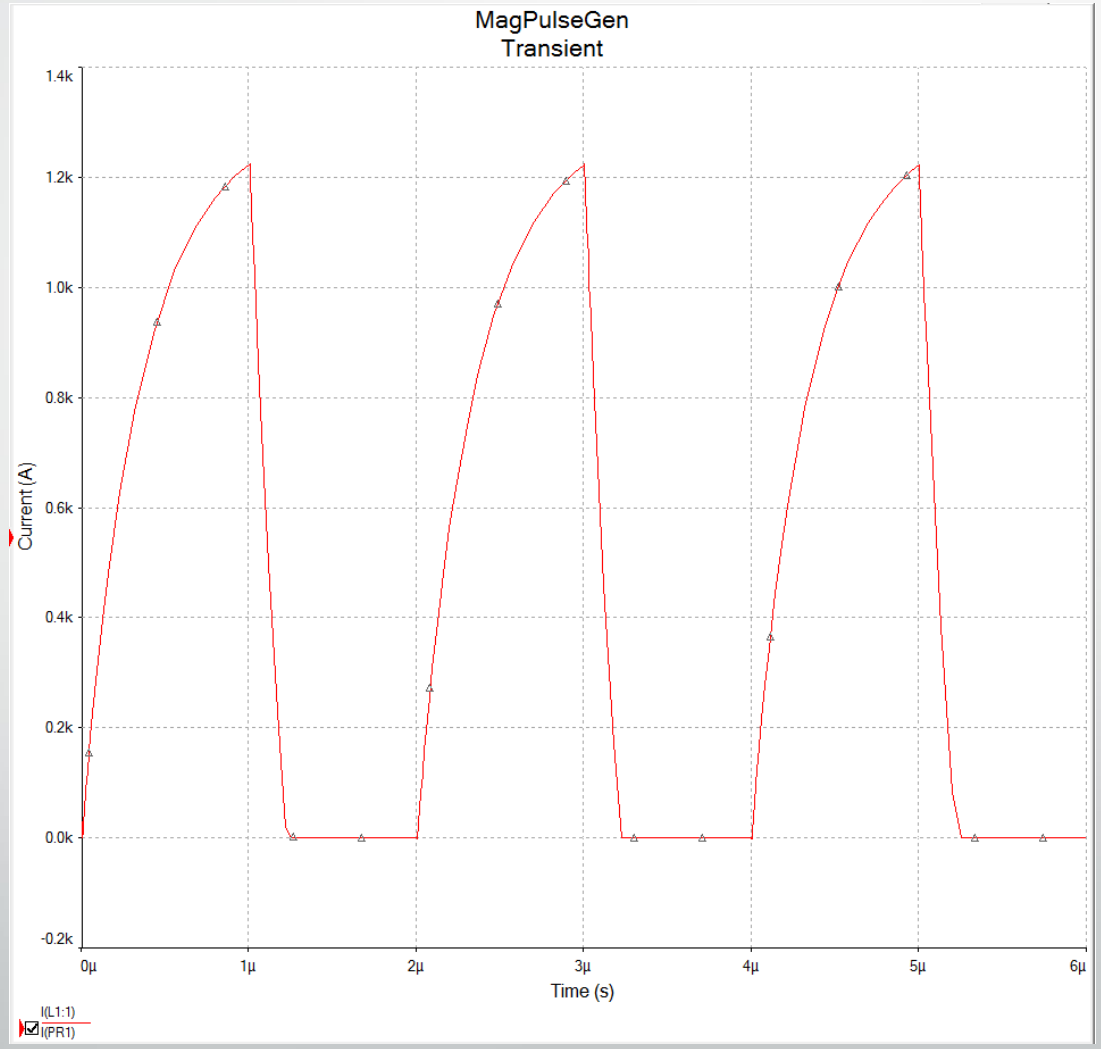
Function Generator setting up

Previous Group Circuit Testing Result



Compare with previous group output, our rise time is too long for our final goal, and our graph is not stable as their group. So this is one of the future goal by modifying our circuit board.

Tests


MagPulseGen
Transient
1.4k
1.2k
1.0k
0.8k
0.6k
0.4k
0.2k
0.0k
-0.2k
Current (A)
0µ
1µ
2µ
3µ
4µ
5µ
6µ
Time (s)
I(L1:1)
I(PR1)

FET Calculations

Condition for saturation in a transistor.

$V_{DS} \geq V_{GS} - V_t$

$V_G = 5V$, $V_S = I_d \times 50\ m\Omega$, $V_t = 1.75$

$V_{DS} = V_D - V_S$, $V_{GS} = V_G - V_S$

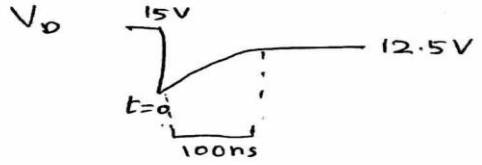
$V_D - V_S \geq V_G - V_S - V_t$

$V_D \geq V_G - V_t$

$V_D \geq 5 - 1.75$

$V_D \geq 3.25V$

We know the shape of voltage at drain.



Rate of change of Voltage at Drain $= \frac{12.5}{100ns}$ (linear approximation for exponential curve) → may not be accurate. But it's okay

$= 0.125\ V/ns$

How long does it take to reach 3.25 V $= \frac{3.25\ V}{0.125\ V/ns} = 26ns$

(≈ 1/4th, rise time)

⇒ Out of 100ns, for 26 ns the transistor is in triode region.

⇒ For $\frac{1}{4}$th of time R_{ds} (ON resistance) $= \frac{1}{K_n (V_{gs} - V_t)}$ → low

≈ 10s of mΩ

For the remaining $\frac{3}{4}$th of time $R_{ds\ ON} = \frac{1}{\lambda K_n (V_{gs} - V_t)^2}$

≈ larger

Source: Jayaprakash

Source Resistor Issues

- Right now, the 0.05 ohm source resistor is only rated for 25 W and the circuit is sending it pulses of about 80 W
- It is surviving (maybe because of such short exposure to high power)

References

1. NXP Semiconductors. (2015). PSMN0R9-30YLD Product Data Sheet [PDF]. Retrieved from http://www.nxp.com/documents/data_sheet/PSMN0R9-30YLD.pdf

2. "EE 333 : Lab." EE 333 : Lab. N.p., n.d. Web. 11 Mar. 2016. http://tuttle.merc.iastate.edu/ee333/info.htm

3. Pritchard, John W., Mani Mina, and Robert J. Weber. "Magnetic Field Generator Design for Magneto-Optic Switching Applications." IEEE Trans. Magn. IEEE Transactions on Magnetics 49.7 (2013): 4242-244. Web.

4. Simple FET DC Bias Circuit (2016) [PDF] Retrieved from http://my.ece.ucsb.edu/York/Bobsclass/2B/Extras/FET%20Biasing.pdf

5. "How Can I Import a SPICE Model Into Multisim?" - *National Instruments*. N.p., n.d. Web. 06 Nov. 2016. http://digital.ni.com/public.nsf/allkb/2373E75D8B375EA1862575D2004D9C88

Razavi, Behzad. *Design of Analog CMIS*. Los Angeles: U of California, 2001. *Https://www.u-cursos.cl/usuario/9553d43f5ccbf1cca06cc02562b4005e/mi_blog/r/[Razavi]_Design_Of_Analog_Cmos_Integrated_Circuits.pdf*. Web. July 2000.

6. Pritchard, John W., Mani Mina, Robert Y. Bouda. "Feel the pulse", Magnetics Technology International, p4-7 (2013). http://viewer.zmags.com/publication/17fdeoad%23/17fdeoad/6

7. "Magnetic Pulse Generator." N.p., n.d. Web. http://dec1622.sd.ece.iastate.edu/

8. Pritchard, John W., Mani Mina, and Narimdinada Y. Bouda. "Feel the Pulse." N.p., n.d. Web. http://viewer.zmags.com/publication/17fdeoad#/17fdeoad/6